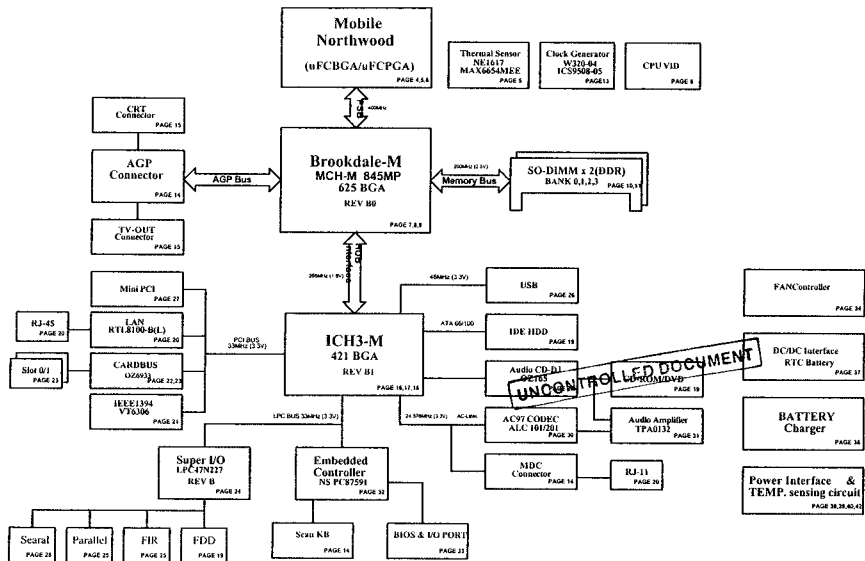


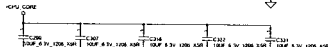
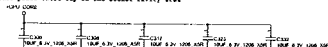
ACL10 LA-1331 BLOCK DIAGRAM



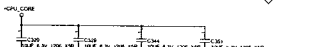
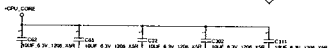
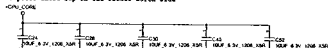
Layout note:

Place capacitors CPU Use 2-3 vias per PAD.
Place 320F high undermount balls on solder side.
Place 100F high on the peripheral near balls.
Use 2-3 vias per PAD.

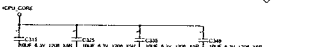
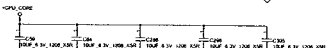
Please place these cap in the socket cavity area



Please place these cap on the socket north side

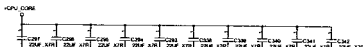
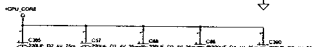
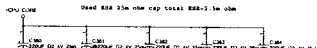


Please place these cap on the socket south side

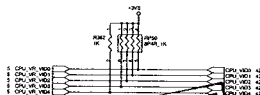


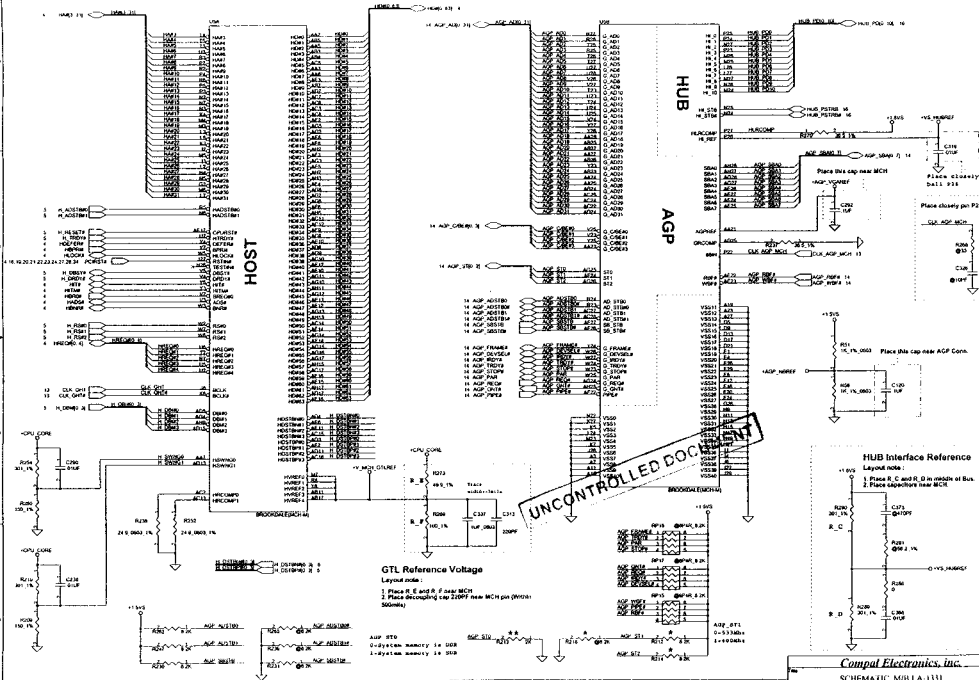
Layout note:

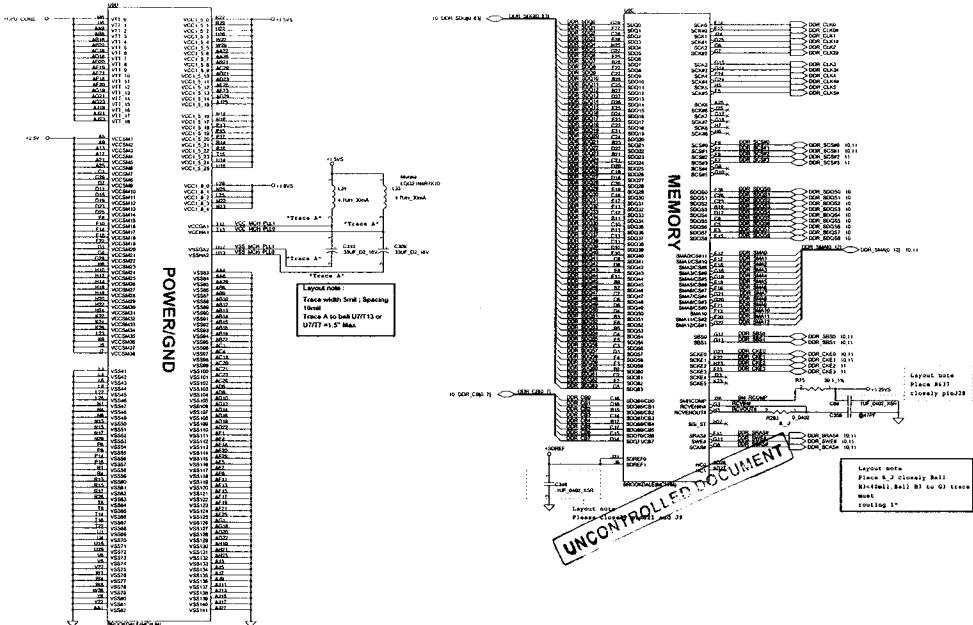
Place close to CPU power and ground pin as possible (10mm)



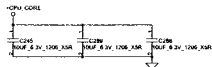
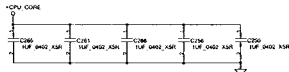
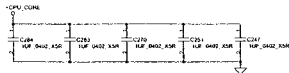
CPU Voltage ID



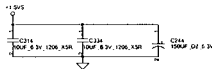
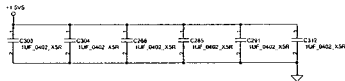




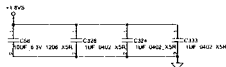
Layout note : Processor system bus
Distribute as close as possible
to MCH Processor Quadrant (between VTTFSB and VSS pin)



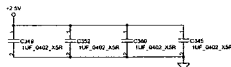
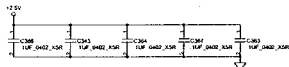
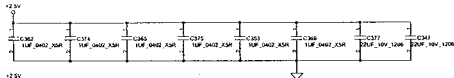
Layout note : AGP/COKE
Distribute as close as possible
to MCH Processor Quadrant (between VCCAGP/VCCORE
and VSS pin)



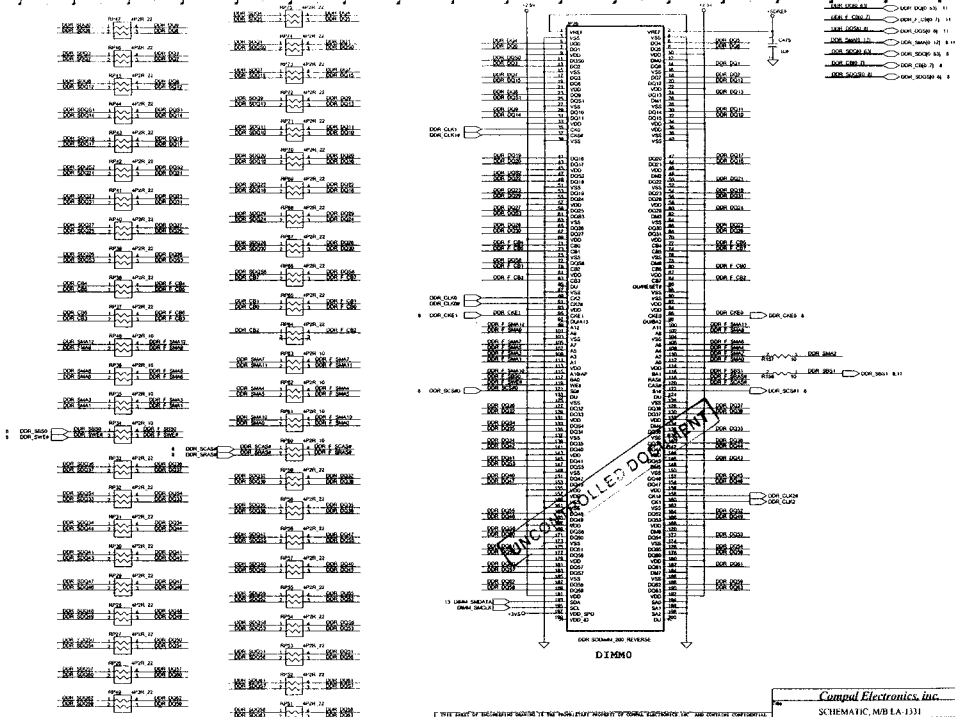
Layout note : Rub-Link
Distribute as close as possible
to MCH Processor Quadrant (between VCCRL and VSS pin)



Layout note : DDR Memory Interface
Distribute as close as possible
to MCH Processor Quadrant (between VCCSM and VSS pin)



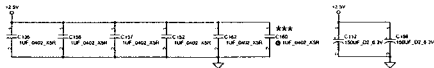
UNCONTROLLED DOCUMENT



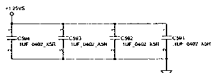
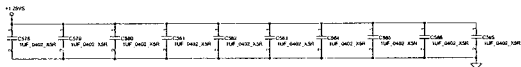
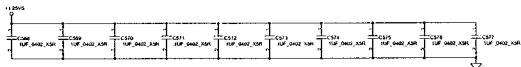
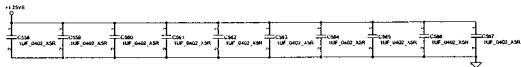
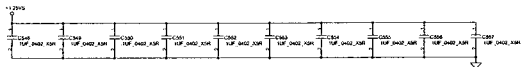
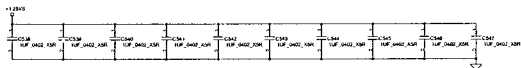
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Layout note:
Place as close as possible
to DCR-SOCMM



Layout note:
Place one cap close to every 2 pull up resistors termination to
+1.25V

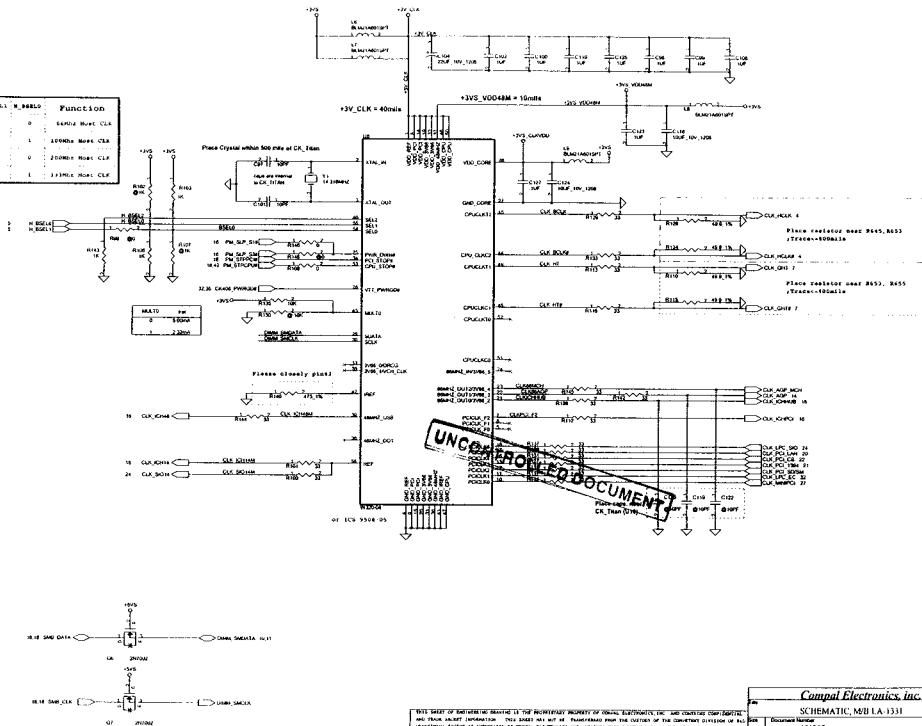


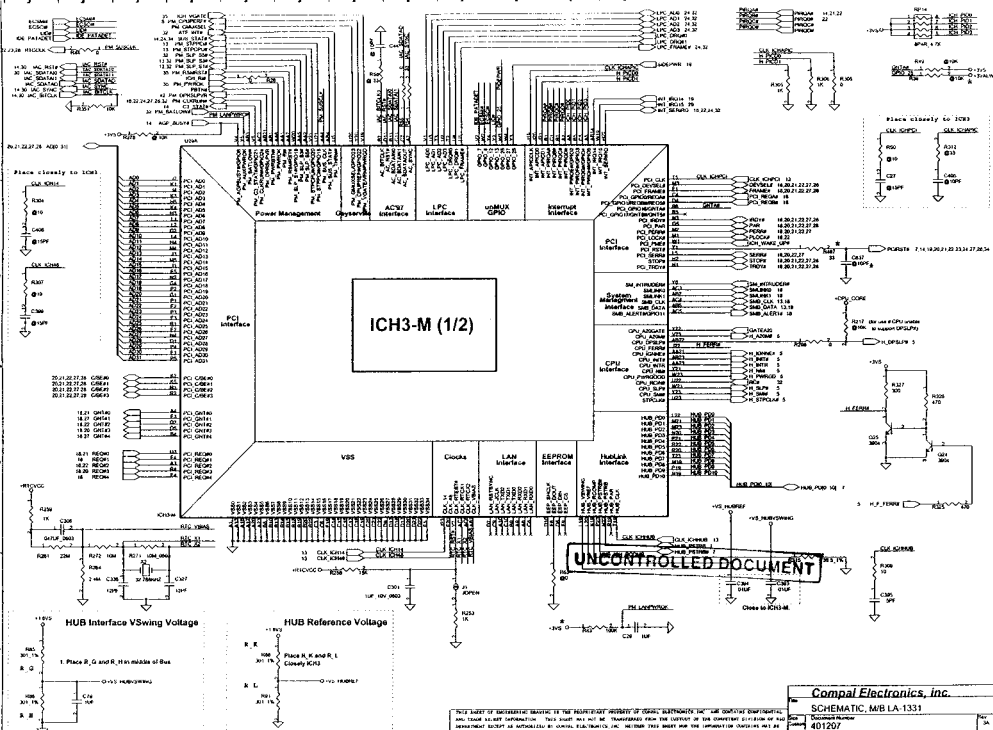
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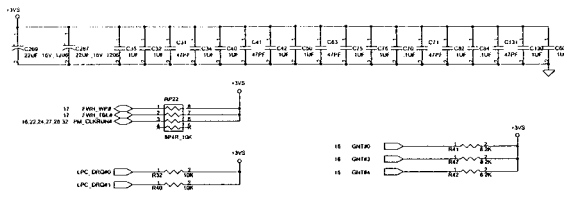
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Compaq Electronics, Inc.	
SCHEMATIC, M/B LA-1331	
Doc #	401207
Rev	12 of 33

N	SHLL	N	SRLO	Function
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★	0	1	0	100MHz Host CLK
	1	0	0	200MHz Host CLK
	1	1	0	300MHz Host CLK

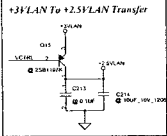




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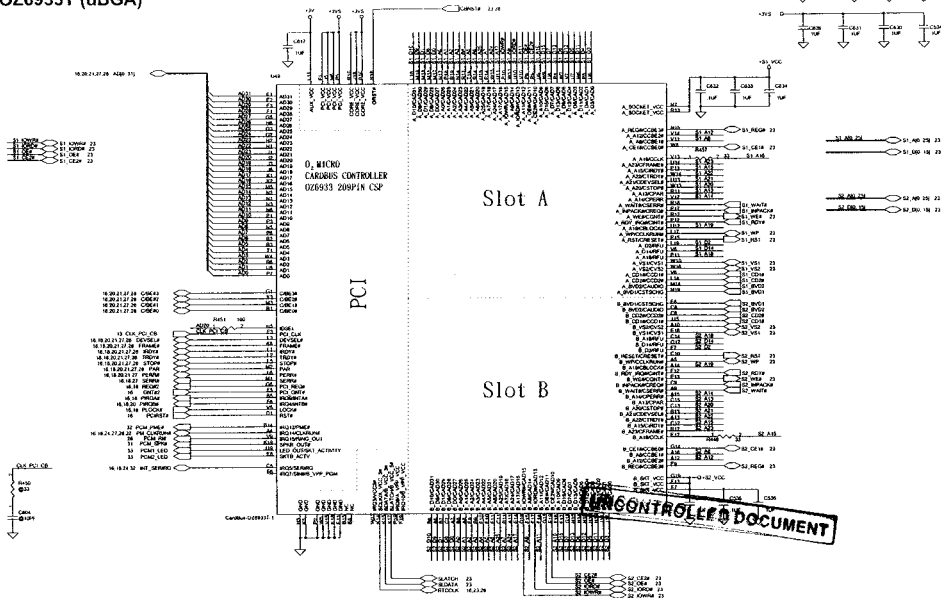
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Compal Electronics, Inc.
Title SCHEMATIC, M/B LA-1331
Doc. Number 401207
Date 9/16/90 Sheet 10 of 31



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CardBus Controller
OZ6933T (uBGA)



UNCONTROLLED DOCUMENT

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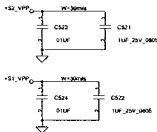
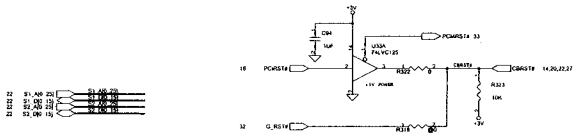
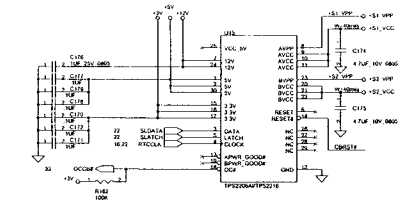
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SCHEMATIC, N/B LA-1331

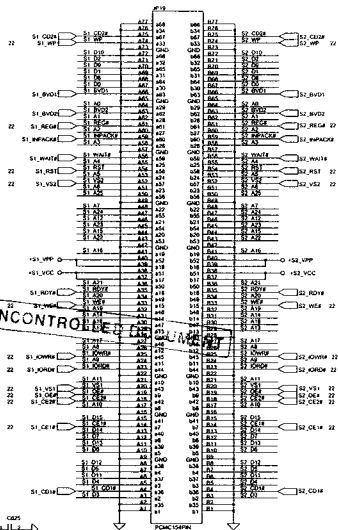
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PCMCIA POWER CTRL.



CARDBUS
SOCKET



UNCONTROLLED

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2009

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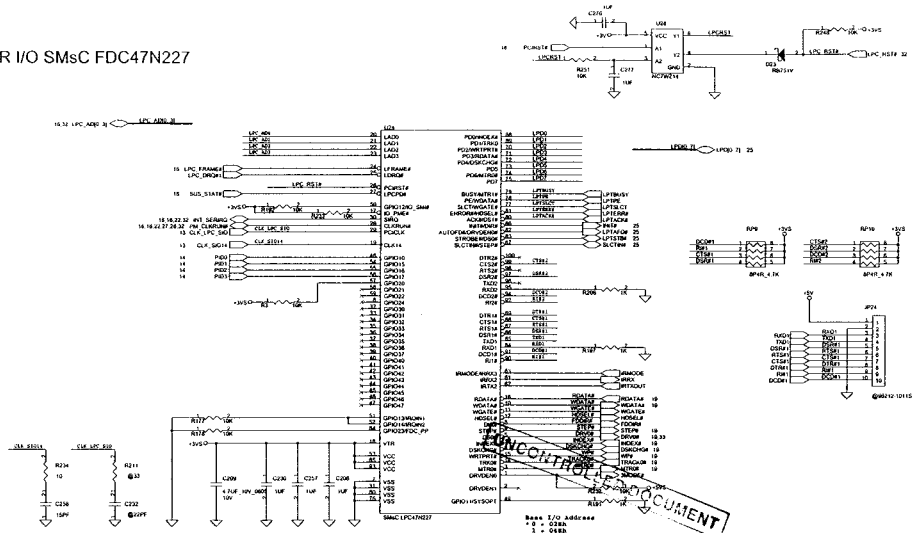
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SUPER I/O SMsC FDC47N227



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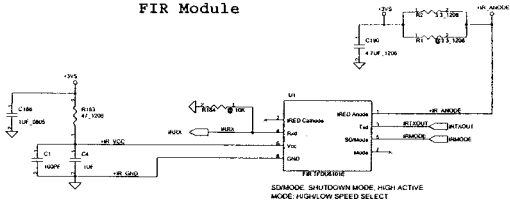
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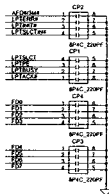
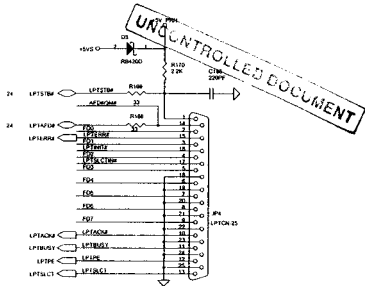
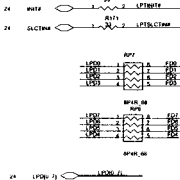
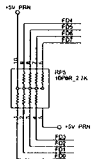
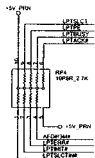
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Expt	24	48	72
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3	0.00	0.00	0.00
4	0.00	0.00	0.00
5	0.00	0.00	0.00
6	0.00	0.00	0.00
7	0.00	0.00	0.00
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FIR Module



PARALLEL PORT



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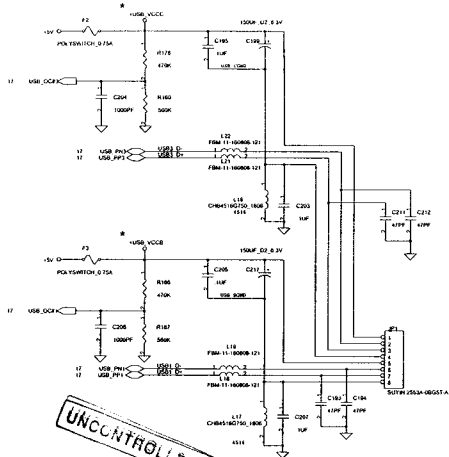
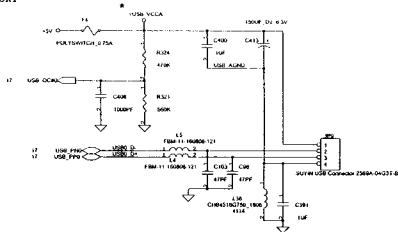
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USB PORT



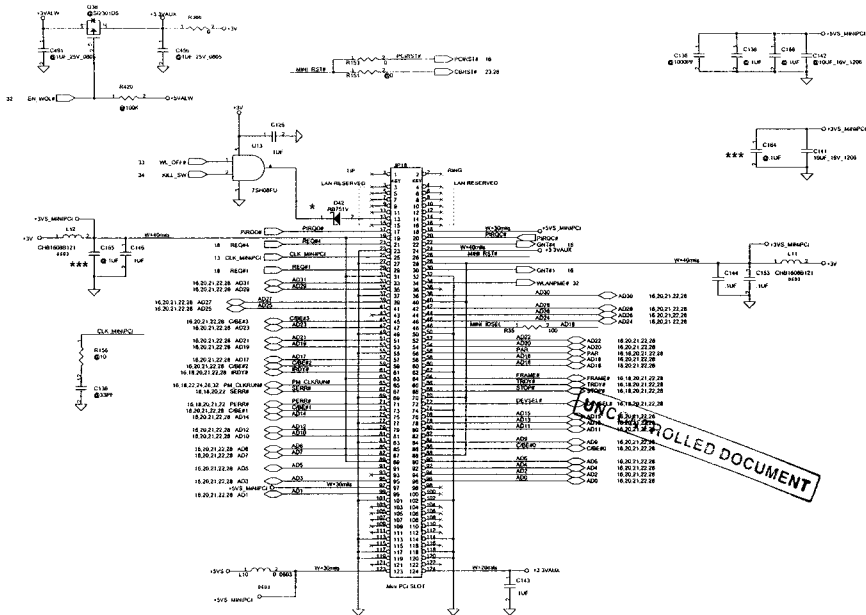
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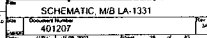
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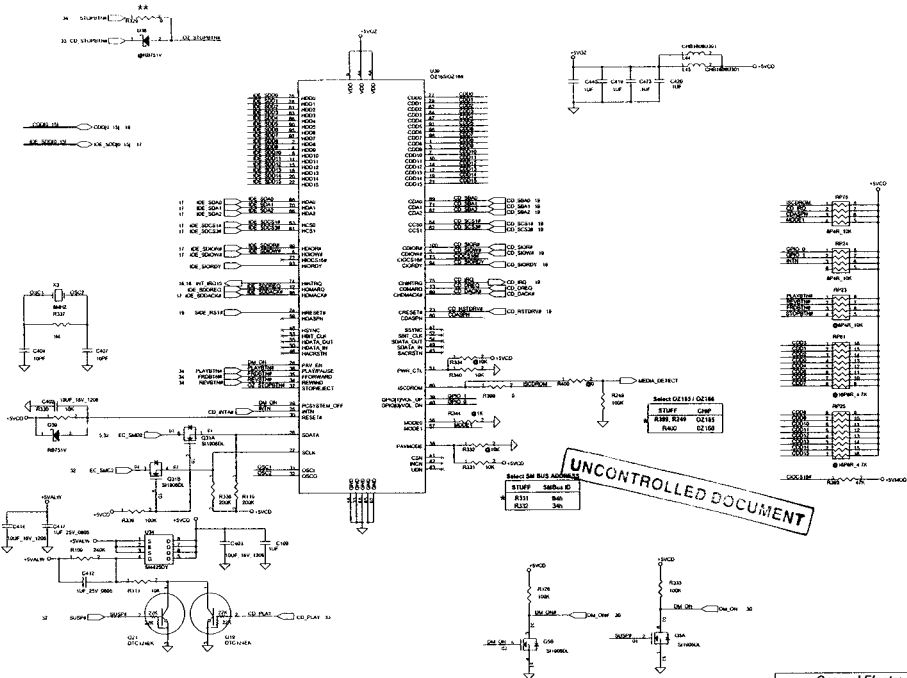
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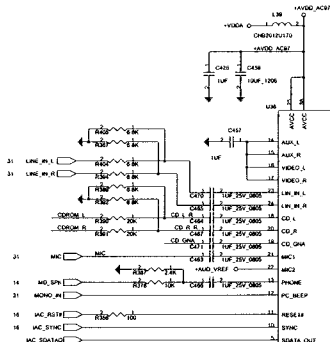
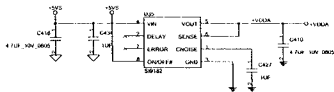




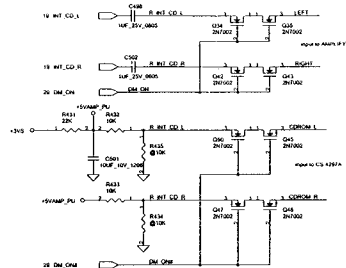
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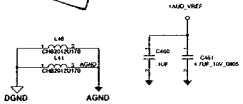
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RT40	MODE
Shift	14.318MHz External
No-Shift	24.576MHz Crystal or External Clock

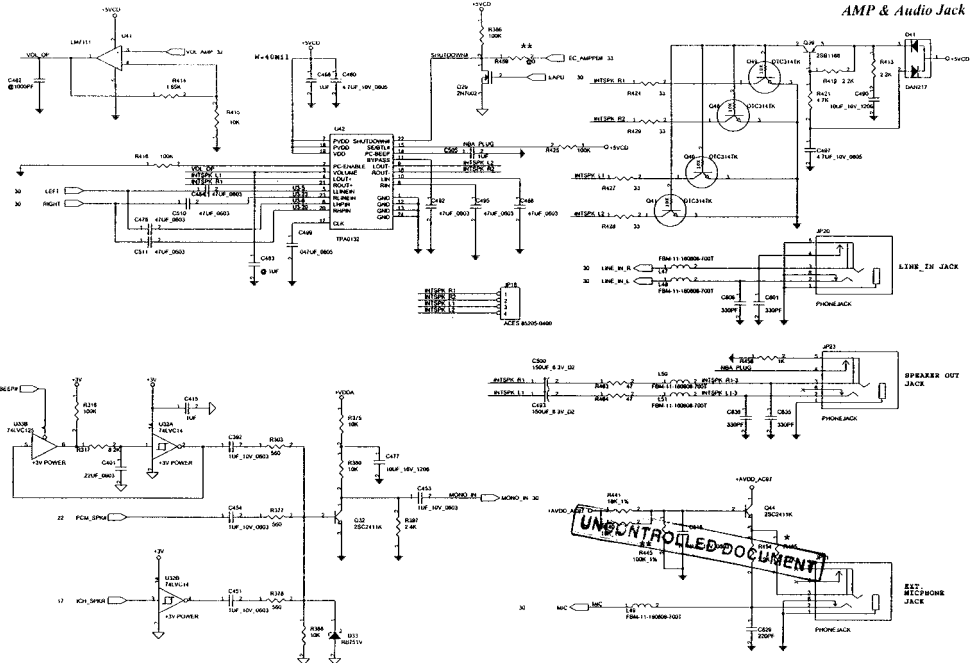


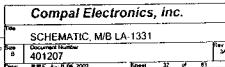
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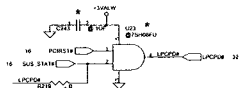
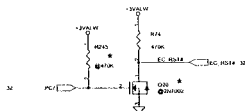


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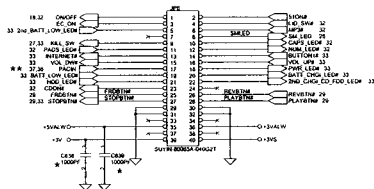
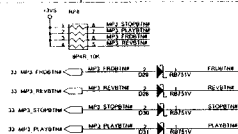
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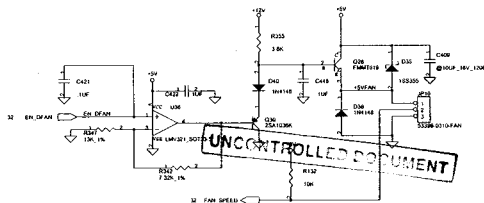




For PC87591 REV 0.A Only



FAN CONN.



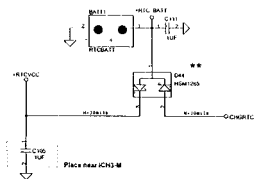
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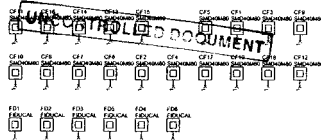
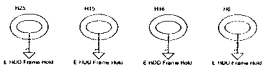
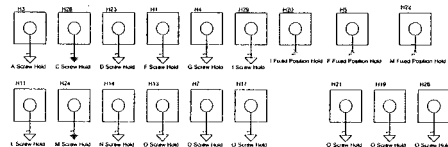
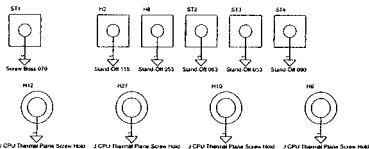
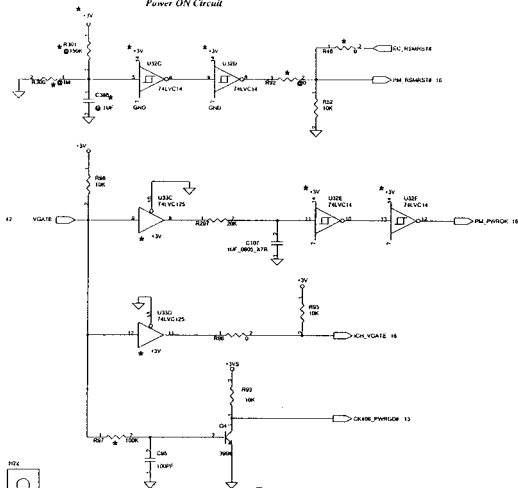
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RTC Batt. Connector



Power ON Circuit



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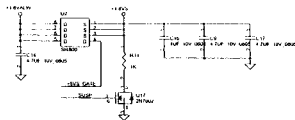
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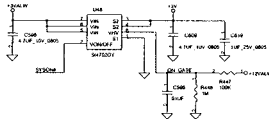
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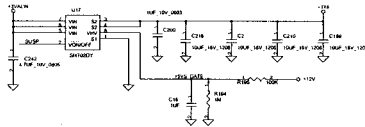
+1.8V_{ALW} To +1.8V_S Transfer



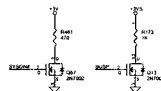
+3V_{ALW} To +3V Transfer



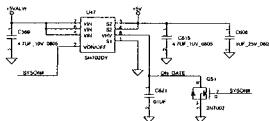
+3V_{ALW} To +3V_S Transfer



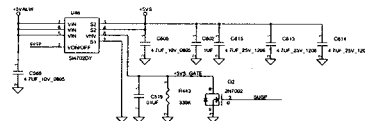
+3V & +3V_S Discharge



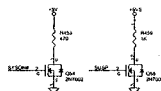
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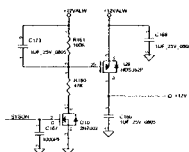
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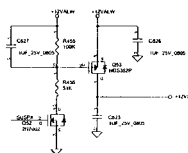
+5V & +5V_S Discharge



+12V_{ALW} To +12V Transfer



+12V_{ALW} To +12V_S Transfer



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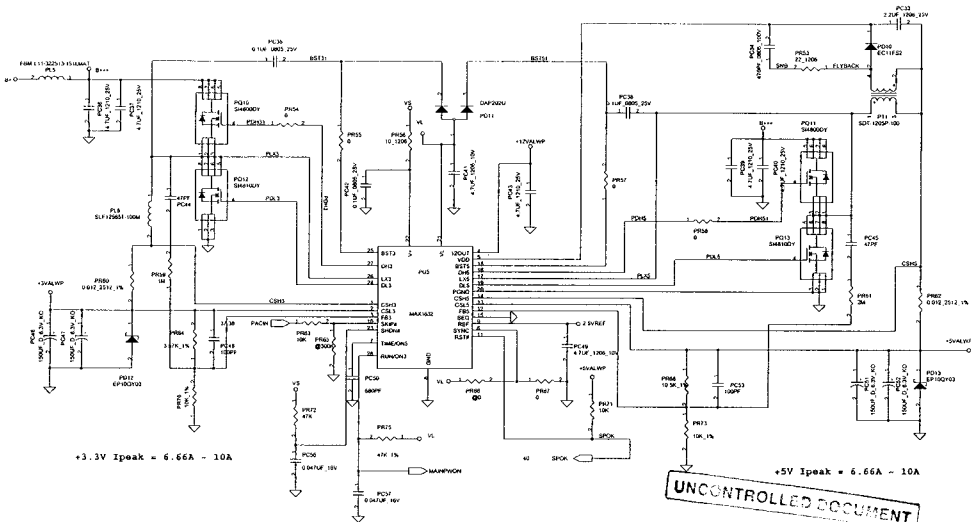
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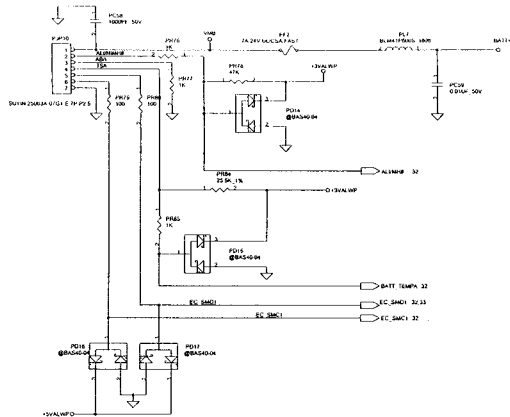


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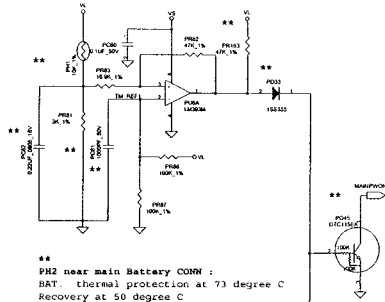
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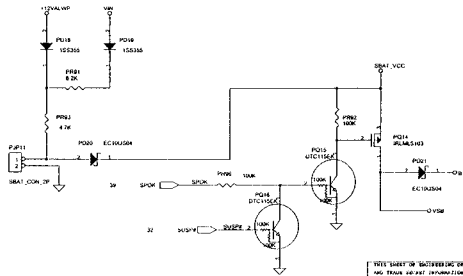
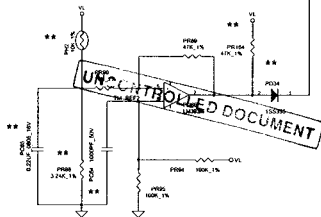


**

PH1 under CPU bottom side :
CPU thermal protection at 87 degree C
Recovery at 48 degree C



PH2 near main Battery CONN :
BAT thermal protection at 73 degree C
Recovery at 50 degree C



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